Introduction to TowerJazz On-Chip ESD Protection

TowerJazz Global Symposium
Newport Beach - October 2010

Roda Kanawati, Avi Parvin, David Quon
**Purpose**

- Highlight key concepts and recommended methodologies to help customers meet their design/product ESD goals.

**Outline**

- Introduction:
  - ESD and using a foundry key protection concepts
- Typical schemes
  - Power Management
  - BiCMOS/RFCMOS
- Q&A
Introduction: ESD and TowerJazz foundry

- Customers need to “own” ESD for their products
  - Be familiar with the ESD schemes, and self-regulate their compliance to guidelines
  - Ultimately learn own lessons about ESD vs product implement. & sustainability.
  - Ask questions, because TowerJazz ESD solutions are diverse, may be unconventional, and usually require some deliberate sizing-up, especially for custom mixed signal apps.

- TowerJazz focuses primarily on HBM/MM ESD:
  - A packaged component’s response to HBM/MM testing is determined primarily by factors on silicon (on-chip), and these can be directly measured at the wafer level using basic foundry-level characterization equipment.
HBM testing evaluates whether a product will survive electro-static discharges from an external capacitor into all combinations of DUT pin-pin pairs. Because of the large 1.5K resistor, 2KV HBM almost always produces a non-oscillatory gaussian discharge waveform with a 150nS FWHM and a peak current of 1.3A.

There is no absolute conversion ratio between MM and HBM, because factors such as DUT impedance and the possibly oscillatory behavior of MM can cause mis-correspondences and different failure mode, but typical product histories and some fundamental equivalences imply that parts passing 4KV HBM should also typically pass 200V MM (20:1).

It’s common to use 100nS square pulses from a Transmission-line-pulser (TLP) to simulate the peak current and power of HBM ESD strikes, and TowerJazz engineering reports may alternatively use TLP instead of HBM data.
Key concepts of on-chip ESD Protection

• ESD protection network
Typical countermeasure for HBM/MM strikes is to shunt any pin-pin discharge with a bypass network that safely sinks excess current while controlling voltages across critical nodes, or to arrange signal paths to themselves be self protecting.

- What can be done to influence a favorable outcome?
- Improve margin $V_{\text{clamp}}$ vs signal path $V_{\text{fail}}$ (use scheme to create a positive ESD window)
- Use adequate metal width and vias in intended discharge paths.
- Follow design and layout practices that improve the ability of the signal and parasitic paths to either withstand higher voltages and currents, or at least avoid weaknesses that can defeat the intended discharge path.
ESD Non-conformity due to package issues and HBM Tester artifacts

Not all HBM/MM product “failures” are due to poor on-chip design.

HBM/MM stressing of N/C pins can setup secondary discharges that are not necessarily HBM events.

These issues could be debugged by excluding N/C pins from ESD test plan, and then controlled by connecting N/C pads to the ESD network instead of leaving them floating.

Some HBM/MM testers can introduce a dc pre-charge on the DUT that may affect the ESD readiness of the protection network to respond to discharges, esp. if power domain has high impedance.

A 10K shunt resistor is permitted during testing. You should check with test vendor, or could add this on-chip.
Typical TS18PM ESD protection scheme

Primary discharge network

- All pads are clamped directly to ground (snapback topology)
  - Snapback devices: ESD NMOS, HV SCR
  - Non-snapback device: HV RC clamp, HV VNP clamp
- Pads may be clamped to supplies if enhancement is required
- All ground busses are coupled with anti-parallel diodes
- MOS Inputs are protected by secondary clamps (CDM)

Enhancements:

- Core devices connected between pads but not directly clamped by ESD device.
  - PMOS of output buffer - Parallel ESD PMOS (to increase failure current)
  - Voltage regulator - Parallel Diode (HV/LV cross domain coupling)
- Core devices behind IO devices (prep. IO devices, drivers to be self protecting)
  - Pre-driver of large output buffer – (should also follow ESD design rules)
  - Driver of LDMOS - Add local clamp (to avoid Vds snapback)
TS18PM LV (cont.): Key Design Requirements

- **All IO’s related with this domain must comply with DR TS18 PM1.**

- **Power IO, either externally or internally generated**
  - Power-clamp based on cgNMOS of minimum size, in full ESD design rules.

- **Input IO**
  - ggNMOS and ESD PMOS of minimum size, in full ESD design rules.
    - Diodes can be added in parallel to ggNMOS and ESD PMOS for higher ESD rating.
  - Secondary ESD between pad and input buffer.
    - All transistor gates which are connected to pad must be done through secondary ESD.

- **Output IO**
  - ggNMOS and ESD PMOS of minimum size, in full ESD design rules.
    - ggNMOS and ESD PMOS, fully or partially, can be used as output-buffer.
    - All transistors with drain connected to pad must be drawn as ESD transistors.
    - When used as output-buffer with over critical size, pre-driver should also be drawn in ESD design rules.
    - Diodes can be added in parallel to ggNMOS and ESD PMOS for higher ESD rating.

- **Power-bussing**
  - Resistance of power/ground bus between IO ESD and nearest power-clamp.
  - Resistance of power and ground bus between two power-clamps.
TS18PM HV Outline

- PM ESD Roadmap
- ESD challenge
- General PM ESD scheme
- Simulation Methodology
- ESD protection devices:
  - RC Clamp (CGNLDMS)
  - SCR (Silicon controlled rectifier)
  - PNP
  - Coupling diodes
ESD Challenge

ESD Challenges:

1. Good Vdd Rdson Tradeoff \((BVDSS-ESD\ design\ window = Vdd)\)
2. Scalable voltage platform \(\rightarrow\) Need scalable ESD voltage solutions
3. Capability to tune ESD Rating.
**General PM ESD Scheme**

**Color legend:**
- Black: ESD devices
- Green: Self protected core devices
- Blue: Core devices which require ESD protection

If the 5V GND and the HV GND have the same potential, then this rail protection could be replaced by 5V anti parallel ESD coupling diodes.
2KV-HBM Spice Simulation

- **tr=tf=1ps**
- **Pulse width=100ps**
- **I=2000 [A]**

**1.5 KOhm**

**100pF**

**100 KOhm**

**10 KOhm**

**nld_5V_sclV**

- **S=4.2 um**
- **Wtot=8,000 um**

**Color legend:**

- Blue-LDMOS Driver
- Green-CMOS pre-driver

**DUT**

Represents floating node during ESD stress.
PM ESD Scheme Example (No Vdd Rail)

Color legend:
- Black-ESD devices
- Blue-Core devices which requires ESD protection

LDNMOS
### TS18PM/TS35PM ESD Protection Devices Comparison

<table>
<thead>
<tr>
<th>Device</th>
<th>Triggering Type</th>
<th>Features</th>
<th>Restrictions</th>
<th>Clamp Size for 40V Application</th>
</tr>
</thead>
</table>
| CGNLDMS  | RC coupled      | • Scalable voltage & ESD rating  
• Predictable ESD performance, using normal operation Spice model | Sensitivity to false triggering due to spike on Power bus (S.R≥1V/ms)          | ~44,000 mm²                                                                                 |
| SCR       | Voltage         | • Scalable voltage & ESD rating  
• High current capability ➔ very small area  
• Fast switching  
• Low capacitance | Low holding voltage ➔ not recommended for power rail protection               | ~9,600 mm²  
For 100mA LU immunity                                                                 |
| Open Base PNP | Voltage       | • Scalable voltage  
• High immunity to false triggering | Large size                                                                  | ~55,000 mm²                                                                                   |
Coupled Gate NLDMOS Clamp (CGNLDMOS)

ESD rating Vs. Wtot

T901847 W#25

V-High

C

Scalable NLDMOS

V-Low

R

TLJ Current [A]

Wtot [μm]

HBM [kV]
CGNLDMOS – PDK Implementation
Silicon Controlled Rectifier (SCR)

X-Section after Diffusion

WTN+WTP

TLP results of HV SCR

Current [A]
0 0.5 1 1.5 2 2.5 3 3.5 4

Voltage [V]
0 10 20 30 40 50 60 70

TLP Current (A)-D1
TLP Current (A)-D2
TLP Current (A)-D3
TLP Current (A)-D4
TLP Current (A)-D5
In order to prevent L/U of the SCR, one should guarantee either: Vh>Vdd or It1 >100mA. Since our SCR’s holding voltage (Vh) is lower than Vdd, we are targeting the triggering current to be higher than 100mA to guarantee L/U immunity.
Open Base PNP (CEO)

Scalable voltage PNP (12v-40v) with ESD rating of HBM>2KV and MM>200v.
HV ESD Diodes

<table>
<thead>
<tr>
<th>Diode type</th>
<th>Size μm² - (dev_area;esd size)</th>
</tr>
</thead>
<tbody>
<tr>
<td>esd_dio_1 (WTN&amp;WTP;Psub)</td>
<td>8,248.2</td>
</tr>
<tr>
<td>esd_dio_2 (PHV/WTN&amp;WTP)</td>
<td>5,060.4</td>
</tr>
</tbody>
</table>

X-Section after diffusion
Summary

- **Base Platform:**
  - **Full Scalable ESD solution:**
    - 1.8v/5v ESD protection
    - 20v-60v CGNLDLDMOS *(RC coupled)*: Ready (PDK3.0 advanced)
    - 20v-60v SCR *(Voltage triggered)*: Ready @ Q4. Currently supported as GDS example, DRC & LVS per customer request
    - 12v-40v PNP *(Voltage triggered)*: Currently supported as GDS example, DRC & LVS per customer request
    - 60v ESD coupling diodes: Ready (PDK3.0)

- **NBL Platforms:**
  - All base platform protections are valid also on the premium platform
## TS18PM (cont.): ESD Verification Checklist (Design Review)

<table>
<thead>
<tr>
<th>Domain</th>
<th>Description</th>
<th>Deliverable</th>
</tr>
</thead>
<tbody>
<tr>
<td>Full-Chip</td>
<td>ESD scheme with highlight of each IO voltage, ESD and core devices which are directly connected to pads</td>
<td>Drawn scheme (PowerPoint, Visio, etc.) &amp; GDS</td>
</tr>
<tr>
<td>5V Domain</td>
<td>All devices which their drain is connected to a pad are drawn with ESD design rules per DR TS18 PM1</td>
<td>Schematics &amp; GDS</td>
</tr>
<tr>
<td></td>
<td>Minimum ggNMOS and ESD PMOS size</td>
<td>Schematics &amp; GDS</td>
</tr>
<tr>
<td></td>
<td>Minimum resistance of power busses between IO and power-clamp</td>
<td>Table of metals, sizes and resistance</td>
</tr>
<tr>
<td></td>
<td>Minimum resistance of power busses between two power-clamps</td>
<td>Table of metals, sizes and resistance</td>
</tr>
<tr>
<td></td>
<td>All transistor gates connected to pad through secondary ESD resistor</td>
<td>Schematics &amp; GDS</td>
</tr>
<tr>
<td>HV Domain</td>
<td>Simulation of RC power-clamp - No node is higher than allowed by DR for given device</td>
<td>Waveform of ESD source current and voltage, internal nodes maximum voltage</td>
</tr>
<tr>
<td></td>
<td>Simulation of self protected IO - No node is higher than allowed by DR for given device</td>
<td></td>
</tr>
</tbody>
</table>

- Survey all pins for voltage travel, signal devices exposed to bonding pads
- Utilize standard devices, follow design rules for layout and connectivity
- Simulate HV solutions to ensure that LDMOS snapback is avoided.
Typical SBC/RFCMOS ESD scheme

- Using rail-based ESD scheme for primary protection network
  - topology
  - devices
  - Meeting voltage clamping performance targets
  - typical design exercise / customer interaction
  - additional design/layout enhancements
SBC (cont.): Rail-based Methodology

**Primary protection Network**
- All power domain rails should be shunted by active bigNPN or bigFET clamps.
- All IO pins should be coupled to the local power/ground by using ESD diodes.
  - Diodes conduct current only in the forward direction (see discharge path)
- Power domains should be “coupled together” to enable arbitrary pin-pin discharge
- *Clamped voltages can be scaled* (should be done deliberately to meet safety targets)

**Example of safety targets to define success criteria:**
- NMOS outputs should use nwell-extension on drain if HBM Vds not controlled < 7V.

**Additional considerations**
- Supporting precautions for design and layout to avoid defeat of protection network.
  - Follow latch-up guard ring guidelines (par-bjt); avoid unbuffered cross-domain signal paths.

**Known Limitations:**
- *Fail safe, IO voltage travel, bigFET/bigNPN power-up delay* – consider snapback soln.
**SBC (cont.): Other viable rail-based topologies**

All topologies are viable, provided voltages across critical nodes are kept at safe values.
TowerJazz recommends using a bigFET or bigNPN transient power-supply clamp for rail-based ESD schemes.

Under dc conditions, the cell behaves as a reverse biased ESD diode between Vcc and gnd.

Under ESD conditions, for positive polarity pulses on Vcc relative to Gnd, the cell behaves as a forward biased ESD diode between Vcc and gnd, for a duration of at least 1uS, provided the initial voltage on the cell is 0V. The “diode” action can be represented by a piecewise linear model consisting of a 1V battery with series resistance.

Hence, the discharge network consists effectively of a network of forward biased diodes coupling all pairs of package pins.
SBC (cont.): p18 ESD diode cross-sections

SBC18 standard ESD diodes are made from 3.3V MOS S/D junctions

There are p+/well and n+/substrate types of devices.

p+/nwell names: esd_diode_well_p5x8_X, X = 1, 2, 3, 4, 6, 8
n_/sub names: esd_diode_sub_p5x8_X, X = 1, 2, 3, 4, 6, 8

Each diode has X multiple junction (hot) fingers, surrounded by tie-downs.
Each diode is enclosed by a peripheral guard ring to collect latch-up current.

Fig. 1.a. Cross-section of single-finger p+/nwell type diode. Anode is hot finger, Cathode is nwell tie-down.

Fig. 1.b. Cross-section of single-finger n+/substrate type diode. Cathode is hot finger and Anode is sub tie-down.

Designers can choose devices to meet their capacitance / ESD needs
SBC (cont.): Using 100nS TLP to characterize devices

A transmission line pulser (TLP) is used to characterize component-level HBM ESD behavior in detail: it acquires IV data using ~100nS wide square pulses.

A fair model for ESD diodes and power supply clamps can be as simple as a battery (Voff) with a series resistor (R). Victim devices can also be characterized by a failure current and voltage.

With this type of data, the response of the dedicated on-chip protection circuit can be predicted and compared to that of alternative signal or parasitic paths.
SBC (cont.): Example Customer Interaction

Given pad ring layout containing primary protection network, (A) insufficient metals/vias can be detected by visual inspection, and (B) a simplified physical netlist can be built for spice simulation, using the above PWL models for devices, and resistors to represent interconnects.

HBM network test ; Time= 5:11:26 PM
* .OPTIONS ITL1=200
testframe netlist
iesd 0 hbm dc 1.3
rhi hbm PAD_POS 1e-6
rlo PAD_TRP 0 1e-6
*
XDESDHFDCFB_VCC PAD_HFDCFB VCC_HFDCFB DESD_4X
XDESDHFDCFB_GND GND_HFDCFB PAD_HFDCFB DESD_4X
R_VCC_HFDCFB_VCC_SWACDC VCC_HFDCFB VCC_SWACDC 0.11
R_GND_HFDCFB_GND_SWACDC GND_HFDCFB GND_SWACDC 0.11
XDESDSWACDC_VCC PAD_SWACDC VCC_SWACDC DESD_4X
XDESDSWACDC_GND GND_SWACDC PAD_SWACDC DESD_4X
R_VCC_SWACDC_VCC_SW50OHM VCC_SWACDC VCC_SW50OHM 0.0675
R_GND_SWACDC_GND_SW50OHM GND_SWACDC GND_SW50OHM 0.0675
XDESDSW50OHM_VCC PAD_SW50OHM VCC_SW50OHM DESD_4X

... 

* ESD components
  .subckt DESD_4X p n
d1 p 1 ideal_desd_4x
  voff 1 n 1 volt
  .ends
  .subckt BIGNPN2S p n
d1 p 1 ideal_bignpn
  voff1 1 2 1 volt
d2 2 3 ideal_bignpn
  voff2 3 n 1 volt
  .ends
  .subckt shunt p n
  r p n 0.01
  .ends
* -----------------------------------
* analysis statements
  .dc iesd 0 1.3 0.1
  .end
SBC (cont.): Design Example Analysis

The PWL netlist can be simulated to confirm that the projected voltage clamping capability of the network is adequate under 2KV HBM (1.3A)

<table>
<thead>
<tr>
<th>IO-Rail Voltage</th>
<th>V</th>
<th>IO-IO voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>roster</td>
<td>x</td>
<td>IO1 7.50</td>
</tr>
<tr>
<td>IO1</td>
<td>5.43</td>
<td>2.02 5.43</td>
</tr>
<tr>
<td>IO2</td>
<td>5.49</td>
<td>2.02 5.49</td>
</tr>
<tr>
<td>IO3</td>
<td>5.58</td>
<td>2.02 5.58</td>
</tr>
<tr>
<td>IO4</td>
<td>5.58</td>
<td>2.02 5.58</td>
</tr>
</tbody>
</table>

- io-gnd: current flows thru fwd-biased io-vcc diode, then from power to ground
- io-vcc: current flows thru single fwd-biased diode
- vcc-io: current flows thru power to ground, then thru fwd biased io-gnd diode
- gnd-io: current flows thru single fwd-biased diode

---

Revised schematics showing power coupling (red) at

---

… or help identify different netlist scenarios that may lead to a better voltage-clamping solution.
SBC (cont.): Common corrections to improve clamping voltage

Basic Principles:

• pin-pin discharge path resistance depends on device and bus resistances.
• conductances of active clamps like bigFETs and bigNPNs add in parallel because they are actively triggered.
• Metals and vias at each critical metal interchange sized for > 2KV HBM

Actions for improving voltage clamping capability of the ESD network:

- Reducing bus resistances
- Using larger or parallel ESD diodes
- Adding more power supply clamps
- Locating power supply clamps closer to IO pads
- closing open domains, or sharing clamps between adjacent domains.
Concepts: Enhancing the Standoff Voltage of Signal Paths

Nwell has super-linear resistance with increasing current density

NFET failure characteristics after Vds snap back: regular nmos and nfet_esd.
Concepts: Enhancing the Maximum Current of Signal Paths

“C” shaped current trajectory focuses higher current thru devices with smaller series resistance.

“S” shaped current trajectory encourages all transistors to conduct current uniformly because series resistance for each device is the same.

Wide metal connection on plain NFET allows current to focus at center of finger, ruining IT2.

Diffusion resistance is believed to create a ballasting effect that makes drain current density uniform along the finger.

Using narrow metal that encourages full utilization of each finger’s width, and weak body ties to encourage the parasitic npn to turn on, can enable NFETs to sink appreciable currents under snapback, and hence use poly resistor for ballasting.
Concepts: Avoiding Parasitic BJT failures

Parasitic npn between bonding pads can introduce severe ESD weakness.

Layout of IO circuitry showing potential weakness attributed to cross-device parasitic npn.

Layout of IO circuitry with cross-device parasitic passivated by substrate tie-down guard ring.

Unpassivated parasitic npn may bypass the NMOS output.

NMOS output is isolated by body tie guard ring.

ESD-relevant schematic of IO circuit with potential weakness due to cross-device parasitic npn.

ESD-relevant schematic of IO circuit with Cross device parasitic passivated by guard ring.
Concepts: Avoiding Cross-Domain Failures

Most ESD protection networks are only intended to clamp voltages within a given power domain, esp. IO to local power or ground.

Vgs of the MOS input above is not necessarily clamped to safe levels because it is determined by multiple cross-domain ESD components and bus resistance.

A typical parasitic npn cross section (left) and IV characteristics (right); dashed lines represent snapback holding voltage. Strong body ties can elevate snapback holding voltage and voltage failure threshold, especially if the emitter is tied to ground. Series resistance will more generally elevate the voltage failure threshold.
SBC/RFCMOS Summary

- **Base platform:**
  - Recommended topology: rail based primary protection network
  - Active rail clamps enable high performance clamping
  - Customer can and should deliberately design network to meet specific voltage clamping targets
  - Customer can follow design and layout practices to assist the primary network